TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.: ITL.0501US

In Re Application Of: **Russell E. Henning**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/751,129	December 29, 2000	Anand S. Rao	21906	2613	9172

Invention: **Providing Error Resilience and Concealment for Video Data**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **November 2, 2004.**

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Dated: **December 15, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Russell E. Henning	Art Unit:	2613
Serial No.:	09/751,129	Examiner:	Anand S. Rao
Filed:	December 29, 2000		
For:	Providing Error Resilience and Concealment for Video Data	Atty Docket:	ITL.0501US P10387

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APPEAL BRIEF

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Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-28 (Rejected).

Claim 29 (Canceled).

Claims 30-33 (Rejected).

Claims 1-28 and 30-33 are rejected and are the subject of this appeal brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1

Claim 1 calls for an apparatus including a first block to process a first type of frame in a video bit stream using a first error resilience technique. Error resilience techniques typically limit the scope of degradations that errors in the compressed video cause in the decoded video stream. See page 8, lines 18-20.

In one embodiment, the first block can be part of the error resilience portion 204 shown in Figure 2. That error resilience portion 204 provides a different error resilience technique for I-type, P-type, and B-type frames. See page 8, lines 14-18. These frames are the three types of frames produced pursuant to the MPEG standards. See page 1, line 24, through page 2, line 16. For example, the block 238 may be used to provide error resilience for I-type frames. See the specification, page 8, lines 18-24. For P-type frames, the error resilience technique may provide data partitioning by a data partitioning block 240, reversible variable length coding by a reversible length code block 242, header extension coding by a header extension code block 244 and resynchronization marking by a resynchronization marker block 246. See the specification at page 8, line 28, through page 9, line 3.

The claim goes on to call for a second block to process a second type of frame in the video bit stream using a second error resilience technique. The first error resilience technique is different from the second error resilience technique. The second error resilience technique is to replace a bit pattern for the second type of frame with a shorter bit pattern. See the specification at page 11, lines 6-16, where it is explained that the VLC or variable length coder block 255 replaces frequently occurring bit patterns with codes of shorter length, thereby reducing the total number of bits to be transmitted.

Claim 3

Claim 3 depends from claim 1 and calls for the second block to comprise a resynchronization marking block. A resynchronization marking block is indicated at 246 and is described in the specification at page 8, line 28, through page 9, line 3.

Claim 10

Claim 10 is an independent claim calling for an article comprising one or more machine readable storage media. The media stores instructions that, when executed, enable a processor to receive a video stream having at least a first type of frame and a second type of frame. The first type of frame is processed using a first error resilience technique and a second type of frame is processed using a second error resilience technique, wherein the first error resilience technique comprises applying resynchronization markers to the video stream at a selected interval and the second error resilience technique comprises applying resynchronization markers at an interval different from the selected interval such that the second error resilience technique replaces a bit pattern for the second type of frame with a bit pattern of shorter length.

Referring to Figure 2, the B-type frames may be processed by a resynchronization marker (RM) block 260, while the P-type frames may be processed by a resynchronization marker block 246. The RM block 260 applies resynchronization markers at a longer interval than that used for P-type frames. See the specification at page 11, lines 16-20.

Claim 11

Claim 11 depends from claim 10 and calls for instructions that, when executed, enable the processor to process a P-type frame using a first error resilience technique.

Claim 12

Claim 12 is dependent on claim 11 and calls for instructions that cause the processor to process a B-type frame using a second error resilience technique.

Claim 13

Claim 13 is dependent on claim 12 and calls for instructions that, when executed, enable the processor to process the B-type frame using a simpler error resilience technique than the P-type frame.

Claim 19

Claim 19 calls for an apparatus comprising a first block to process a first type of frame in an encoded bit stream using a first error concealment technique and a second block to process a second type of frame in the encoded video bit stream using a second error concealment technique wherein the first error concealment technique is different from the second error concealment technique. However, claim 19 goes on to call for the second error concealment technique to copy data lost from a previous second type of frame. In the specification, the RVLC block 242 allows the receiving telecommunications device to recover more DCT coefficient data from a corrupted texture partition. See page 10, lines 3-5.

Claim 27

Claim 27 calls for an apparatus including a first block to perform error concealment on an encoded video signal and provide an output signal. A second block determines at least one channel characteristic. In one embodiment, the error-resilience modifier 500′ determines one or more transmission characteristics of the channel over which data will be transmitted as indicated at 720 in Figure 7. A third block performs error resilience on the output signal based on the at least one channel characteristic.

For example, a signal-to-noise ratio of the one or more channels may be measured. The error resilience modifier 500′ determines at 730 if the current frame is a B frame and, if so, then the EC portion 410 performs error concealment on the B frame using VLD and EC block 435, 440. The ER portion 204 of the error resilience modifier 500′ performs (at 750) error resilience on the B-type frame based on the retransmission channel characteristics using, in one embodiment, the VLC block 255 and the RM block 260. See page 20, lines 3-11.

Thus, in one embodiment, the complexity of the error resilience technique may depend on the signal-to-noise ratio of the communication channel, for example. That is, a noisier channel may call for a more robust error resilience technique, while a relatively noiseless channel may not require much resilience, if at all. For modifying the error resilience of B-type frames, in one embodiment, computationally less complex error concealment and resilient techniques (as compared to techniques for P-type frames) may be used. See page 20, lines 11-20.

The claim goes on to call for the third block to perform error resilience on a first type of frame using a first technique and a second type of frame using a second technique, such as the error resilience technique to replace a bit pattern for the second type of frame with a shorter length bit pattern.

* * *

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Are Claims 1-2, 6-8, 19-23, 25-28, and 30-33 Unpatentable Over Sun in View of Shiomoto?**

B. **Are Claims 3-5, 9, and 24 Unpatentable Over Sun in View of Shiomoto and Further in View of Webb?**

C. **Are Claims 10-18 Unpatentable Over Sun in View of Shiomoto and Webb?**

ARGUMENT

A. Are Claims 1-2, 6-8, 19-23, 25-28, and 30-33 Unpatentable Over Sun in View of Shiomoto?

1. Claim 1

Claim 1 calls for a second block to process a second type of frame in the video bit stream using a second error resilience technique, wherein the first error resilience technique is different from the second error resilience technique such that the second resilience technique replaces a bit pattern for the second type of frame with a bit pattern of shorter length.

The Sun reference fails to disclose the use of first and second error resilience techniques with the respective first and second blocks, as noted by the Examiner. It is suggested that the Shiomoto reference discloses an error concealment apparatus with differing error resiliency techniques based differing code strings in order to re-enforce error-correcting abilities.

There is no teaching of a second error resilience technique which replaces a bit pattern for the second type of frame with a shorter length code. Therefore, the Sun and Shiomoto references, whether considered together or separately, fail to render claim 1 limitations *prima facie* obvious to one of an ordinary skill in the pertinent art. Accordingly, the Section 103 rejection of claim 1 should be reversed.

2. Claim 19

Claim 19 includes a second block to process a second type of frame in the encoded video bit stream using a second error concealment technique, wherein the first error concealment technique is different from the second concealment technique such that the second error concealment technique copies the lost data from a previous second type of frame. The combination of the Sun and Shiomoto references fails to teach or suggest all the limitations of claim 19 as a whole.

Therefore, claim 19 is patentably distinguishable over the cited art. Thus, the rejection of claim 19 should be reversed.

3. Claim 27

Claim 27 calls for a first block to perform error concealment and a second block to determine at least one channel characteristic. A third block performs error resilience on the output signal provided from the first block based on at least the one channel characteristic and provides a modified video signal. The third block performs error resilience on a first type of frame using a first technique and on a second type of frame using a second technique, such that the second error resilience technique replaces a bit pattern for the second type of frame with a shorter length bit pattern.

Thus, for the reasons set forth with respect to claim 1, claim 27 is also patentable. Moreover, there is no teaching of using a second block to determine a channel characteristic and a third block to perform error resilience on the output signal from the first block based at least on that channel characteristic and, further, there is no third block to provide a modified video signal.

B. Are Claims 3-5, 9, and 24 Unpatentable Over Sun in View of Shiomoto and Further in View of Webb?

The apparatus of claim 3 calls for a second block that comprises a resynchronization marking block. The Examiner acknowledges that the Sun and Shiomoto reference combination fails to disclose the use of application of resynchronization markers. However, the Examiner cites to the Webb reference for this teaching.

Webb merely teaches a different recording technique for RVLC for reversible variable length code words of a type implemented for H.263++ and MPEG-4 standards. This method for RVLC decoding by Webb fails to indicate use of a resynchronization marking block where different error resilience techniques for different types of frames are used. Absent this teaching, the Webb reference in combination or separately, with the Sun and Shiomoto references fails to teach or suggest claim 3. Accordingly, the Section 103 rejection of claim 3 should be reversed.

C. Are Claims 10-18 Unpatentable Over Sun in View of Shiomoto and Webb?

Claims 10-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Sun reference in view of the Shiomoto and Webb references. However, the Sun reference, even incorporating the Shiomoto's differing error resiliency techniques for the first and second type of frames, fails to disclose all the limitations of claim 10, as amended absent a teaching for

resynchronization markers application. Thus, the Examiner is respectfully requested to allow claim 10 and the claims depending therefrom. The Examiner is respectfully requested to consider all pending claims.

Shiomoto does not teach using different concealment techniques for P-type and B-type frames as set forth in claims 11-13. The material cited at the bottom of column 8 and the top of column 9 in no way indicates B-type and/or P-type frames are subject to different error resilience techniques.

Respectfully submitted,

Date: December 15, 2004

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CLAIMS APPENDIX

The claims on appeal are:

1. An apparatus, comprising:

a first block to process a first type of frame in a video bitstream using a first error resilience technique; and

a second block to process a second type of frame in the video bitstream using a second error resilience technique, wherein the first error resilience technique is different from the second error resilience technique, the second error resilience technique to replace a bit pattern for the second type of frame with a shorter bit pattern.

2. The apparatus of claim 1, wherein the first block further processes a third type of frame.

3. The apparatus of claim 1, wherein the second block comprises a resynchronization marking block.

4. The apparatus of claim 3, wherein the second block comprises a variable length coder block.

5. The apparatus of claim 1, wherein the first block applies resynchronization markers to the video bitstream at a first interval and the second block applies resynchronization markers to the video bitstream at a second interval, wherein the second interval is longer than the first interval.

6. The apparatus of claim 1, wherein the second block inserts fewer error resilience bits in the video bitstream than the first block.

7. The apparatus of claim 1, further comprising a third block to process the P-type frame using a first error concealment technique.

8. The apparatus of claim 7, further comprising a fourth block to process the second type of frame using a second error concealment technique, wherein the first error concealment technique is different from the second error concealment technique.

9. The apparatus of claim 1, wherein the first block comprises:

a data partitioning block having an input terminal and an output terminal;

a reversible variable length coder block having an input terminal and an output terminal, wherein the output terminal of the data partitioning block is coupled to the input terminal of the reversible variable length code block;

a header extension code block having an input terminal and an output terminal, wherein the output terminal of the reversible variable length code block is coupled to the input terminal of the header extension code block; and

a resynchronization marker block having an input terminal and an output terminal, wherein the output terminal of the header extension code block is coupled to the input terminal of the resynchronization marker block.

10. An article comprising one or more machine-readable storage media containing instructions that when executed enables a processor to:

receive a video stream having at least a first type of frame and a second type of frame; and

process the first type of frame using a first error resilience technique and the second type of frame using a second error resilience technique, wherein the first error resilience technique comprises applying resynchronization markers to the video stream at a selected interval and the second error resilience technique comprises applying resynchronization markers at an interval different from the selected interval such that the second error resilience technique replaces a bit pattern for the second type of frame with a bit pattern of shorter length.

11. The article of claim 10, wherein the instructions when executed enable the processor to process a P-type frame using the first error resilience technique.

12. The article of claim 11, wherein the instructions when executed enable the processor to process a B-type frame using the second error resilience technique.

13. The article of claim 12, wherein the instructions when executed enable the processor to process the B-type frame using a simpler error resilience technique than the P-type frame.

14. The article of claim 13, wherein the instructions when executed enable the processor to insert resynchronization markers in the video stream at a first pre-selected interval for the B-type frame and at a second pre-selected interval for the P-type frame, wherein the first pre-selected interval is longer than the second pre-selected interval.

15. The article of claim 10, wherein the instructions when executed enable the processor to process the first type of frame using a first error concealment technique and the second type of frame using a second error concealment technique, wherein the first error concealment technique is different from the second error concealment technique.

16. The article of claim 10, wherein the instructions when executed enable the processor to insert fewer error resilience bits into the video stream for the B-type frame than for the P-type frame.

17. The article of claim 10, wherein the instructions when executed enable the processor to perform variable length coding on the B-type frame.

18. The article of claim 10, wherein the instructions when executed enable the processor to apply resynchronization markers to the video for the B-type frame.

19. An apparatus, comprising:

a first block to process a first type of frame in an encoded bitstream using a first error concealment technique; and

a second block to process a second type of frame in the encoded video bitstream

using a second error concealment technique, wherein the first error concealment technique is different from the second concealment technique such that the second error concealment technique copies data lost from a previous second type of frame.

20. The apparatus of claim 19, wherein the second block comprises a variable length decoder block.

21. The apparatus of claim 19, wherein the second error concealment technique comprises performing a block copy.

22. A method comprising:

receiving a video stream;

performing error resilience on a first type of frame within the video stream using a first technique; and

performing error resilience on a second type of frame within the video stream using a second technique, wherein the first technique is different from the second technique such that the second error resilience technique replaces a bit pattern for the second type of frame with a shorter length bit pattern.

23. The method of claim 22, further comprising performing error resilience on an I-type frame.

24. The method of claim 22, wherein the first technique comprises applying resynchronization markers to the video bitstream at a first interval and the second technique comprises applying resynchronization markers at a second interval, wherein the second interval is longer than the first interval.

25. The method of claim 22, wherein the second technique inserts fewer error resilience bits in the video bitstream than the first error resilience technique.

26. The method of claim 22, further including performing error concealment on the first type of frame using a first technique and performing error concealment on the second type of frame using a second technique, wherein the first technique is different from the second technique.

27. An apparatus, comprising:

a first block to perform error concealment on an encoded video signal and provide an output signal;

a second block to determine at least one channel characteristic; and

a third block to perform error resilience on the output signal based on the at least one channel characteristic and provide a modified video signal, wherein the third block performs error resilience on a first type of frame using a first technique and on a second type of frame using a second technique such that the second error resilience technique to replace a bit pattern for the second type of frame with a shorter length bit pattern.

28. The apparatus of claim 27, further comprising at least of a block to transmit the modified signal and to store the modified signal to a storage device.

30. The apparatus of claim 27, wherein the first block performs error concealment on a P-type frame using a first technique and on a B-type frame using a second technique, wherein the first technique is different from the second technique.

31. The apparatus of claim 1 wherein said first type of frame is a P-type frame and said second type of frame is a B-type frame.

32. The apparatus of claim 2 wherein said third type of frame is an I-type frame.

33. The apparatus of claim 19, wherein said first type of frame is a P-type frame and said second type is a B-type frame.